

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7182	conver\$7 adj format	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 20:58
L2	22945	SDRAM or (synchronous adj dynamic adj random adj access) or DDR or (double adj data adj rate) or rambus	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 20:59
L3	6044	PCI same SCSI	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 20:59
L4	633	PCI adj controller	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:00
L5	3066	PCI adj interface	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:00
L6	92	upper adj address adj bit	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:00
L7	24901	register adj (block or set or file)	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:01
L8	37076	address with (range or region)	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:02
L9	5	1 and 2 and 3	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:06
L10	0	1 and 2 and 4	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:02

L11	19	1 and 2 and 5	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:12
L12	1	5 same 6	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:11
L13	7	5 and 6	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:03
L14	5	6 and 7 and 8	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:03
L15	0	6 and 11	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:12
L16	16	7 and 11	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:14
L17	16	8 and 16	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:13
L18	82	(memory adj card) same (PCI adj interface)	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:15
L19	33	(memory adj card) with (PCI adj interface)	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:15
L20	1	1 and 19	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:16
L21	12	2 and 19	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:30

L22	1	6 and 19	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:16
L23	1	7 and 19	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:16
L24	6	8 and 19	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:17
L25	1493	(711/167).CCLS.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:30
L26	1905	(711/170).CCLS.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:30
L27	869	(711/173).CCLS.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:30
L28	2	(PCI and controller and memory and address adj bit and convert\$5).clm.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/07 21:31